FB2M5LVR

250 Mbps Fiber Optic LC Transceiver

Data Sheet

DESCRIPTION

The Firecomms LC transceiver features a small form factor housing, compliant with IEC 61754-20. This device offers engineering teams a compact LC interconnect supporting Fast Ethernet, Industrial Ethernet (e.g. EtherCAT and Sercos III) and proprietary data links running data from 10 Mbps up to 250 Mbps. It integrates with the 200 Mbps (8B/10B) port on many FPGA and ASIC devices.

The transceiver includes an integrated transmitter and receiver pair of opto-electrical components, lensed for termination to Plastic Optical Fiber (POF). The LC system offers a compact termination ideal for applications requiring robust plug retention and endurance against vibrations and mechanical shock.

This LC transceiver can be interfaced to low voltage differential data systems (LVDS, LVPECL and CML) for integration into existing data bus structures. For low power and green designs, the transceiver provides an electrical power saving feature. If no data or toning inputs are present on the input bus, the transmitter driver IC will enter a sleep state and the RCLED (Resonant Cavity LED) is switched off. Similarly, with no optical signal present, the receiver IC will switch into a sleep mode. In sleep mode the total power consumption is reduced to a typical value of 27 µA.

The plugs and cable assemblies are also available directly from Firecomms and its distribution partners.

AVAILABLE OPTIONS

Table 1
ORDERING INFORMATION / PART NUMBERS

Industrial LC Transceiver, 2.2 mm POF, Black	FB2M5LVR

FEATURES

- Reliable LC housing with a “click-lock” connection
- Enhanced design for industrial applications
- Compatible with 8B/10B encoding schemes: 250 Mbps is the NRZ symbol rate
- Resonant Cavity LED (RCLED) at red 650 nm with small emission aperture suitable for POF
- Integrated CMOS driver IC for RCLED
- High sensitivity CMOS receiver IC and PIN diode
- Integrated optics for efficient coupling
- Low power consumption with power saving features
- 3.3V operation
- -40 °C to +85 °C operating range
- RoHS compliant

APPLICATIONS

Table 2
APPLICATIONS

Application	Industrial Networking Robotic Links Medical Data Systems Transportation System Buses
Standard	LVDS Bus
Distance	50 meters at 250 Mbps, 0.5 NA Step Index POF [1]
Speed	Up to 250 Mbps

Note: 1. Depending on the installation conditions and data rate, e.g. 80 meters at 125 Mbps Ethernet (point to point

SPECIFICATIONS

Table 3
TRANSCEIVER PIN DESCRIPTION

Pin	Name	Symbol
	Transmitter	
1	EMI Shield [1]	GND
2	Signal Input (Negative)	TD-
3	Signal Input (Positive)	TD+
4	Ground Pin [1]	GND
5	DC Power Input Pin 3.3 V	Vcc
6	Ground Pin [1]	GND
	Receiver	
7	DC Power Input Pin 3.3 V	Vcc
8	Ground Pin [1]	GND
9	Signal Detect Output	SD
10	Data Output (Negative)	RD-
11	Data Output (Positive)	RD+
12	EMI Shield [1]	GND

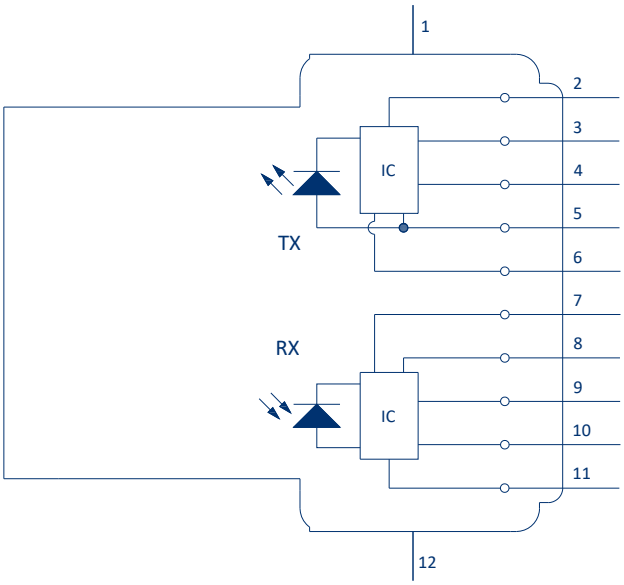

FIGURE 1
Transceiver pin-out, top view

1. NB: EMI Shield ground pins must be connected to the signal ground plane on the PCB. This is important to prevent cross-talk between TX and RX and also to shield the FOT's from external EMI/EMC and ESD

ELECTRICAL INTERFACE

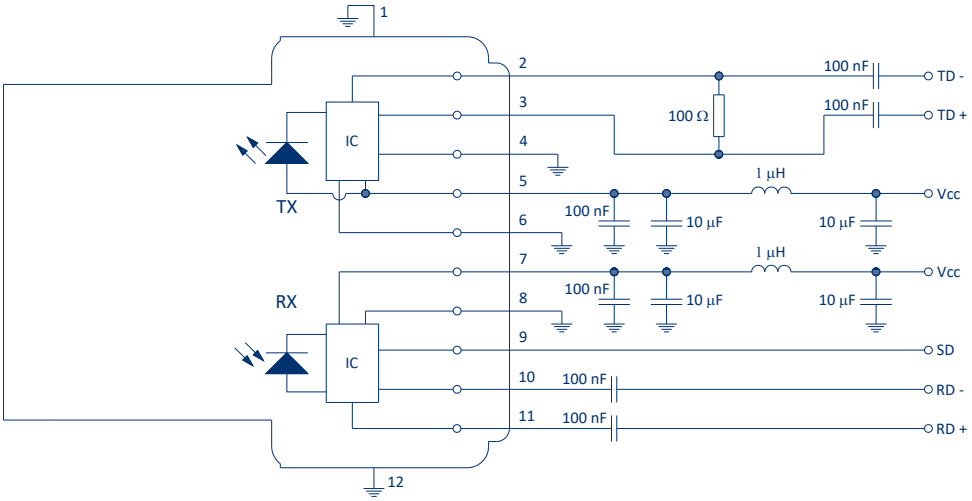

FIGURE 2
Recommended interface to AC couple to an LVDS based PHY.

Notes:

1. *The transmitter (TX) and receiver (RX) are electrically shielded from each other to prevent crosstalk. To be effective this shield must be grounded*
2. *Both GND pins of the TX FOT must be connected to GND (they are not connected internally).*
3. *Power line capacitors should be located as close as possible to the FOT's DC power PINs.*
4. *The data lines are impedance-matched differential pairs. The PCB layout for these tracks must comply to IEEE standards for high-speed data and impedance matching. The 100 nF coupling capacitors are sized for high speed data (100 to 250 Mbps).*
5. *The RD + and RD – lines are already terminated with a 100 Ω resistor internally at the output stage*

ELECTRONIC BLOCK DIAGRAM

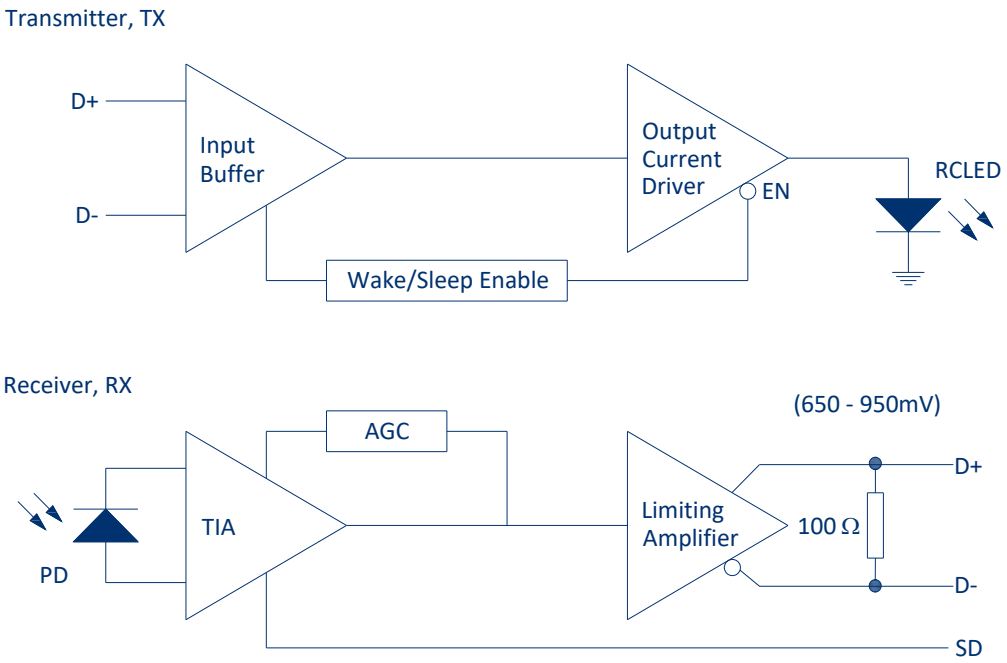

FIGURE 3
Electronic block diagrams of the TX and RX fiber optic transceivers

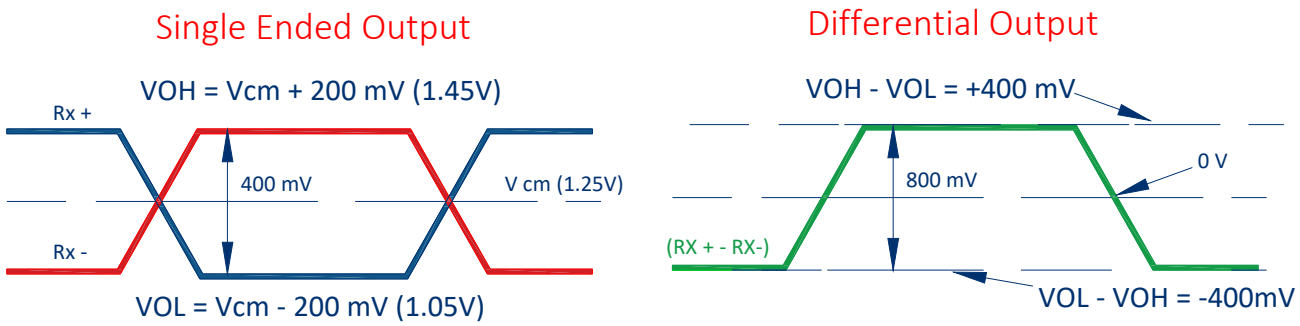

FIGURE 4
On the left the Optical Receiver Output voltage swing as seen from each output (single ended) and on the right as the differential measurement across both outputs.

The overall VOH and VOL values depend critically on the common mode DC level. In LVDS applications this is 1.25V. In LVPECL it is 2V and in CML it is 1.5V. The following application circuits illustrate how the Firecomms part can be used with LVPECL, LVDS and CML interfaces generally found on Ethernet PHY, FPGA and ASIC devices. The specific circuit for an individual manufacturer sometimes differs from these general guidelines. Please contact Firecomms for assistance with specific IC's.

APPLICATION CIRCUIT FOR AN LVDS INTERFACE

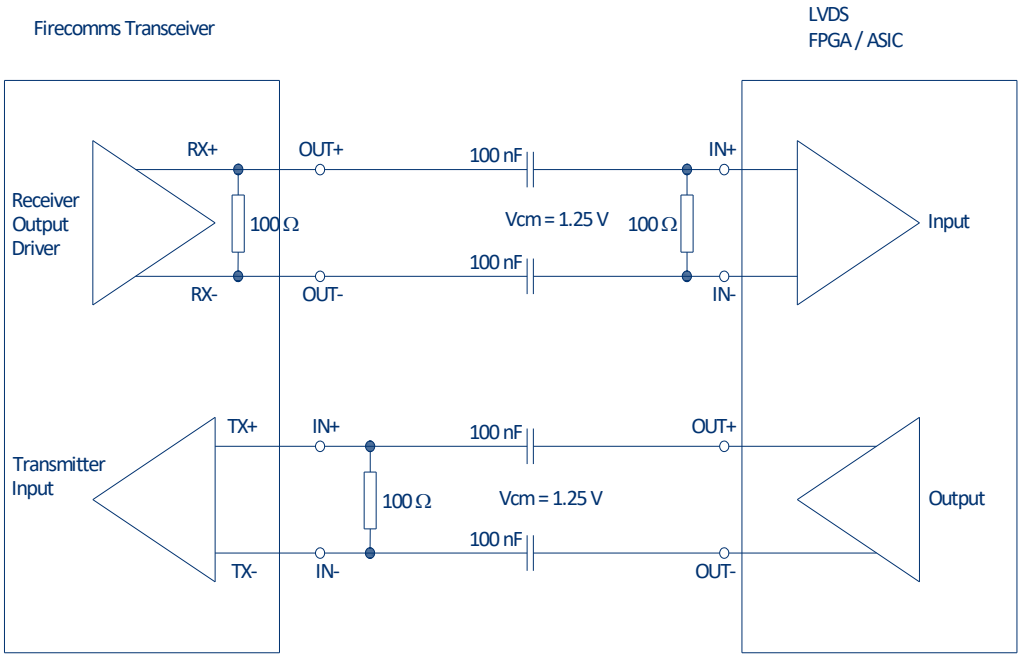

FIGURE 5
This is the general AC coupled LVDS interface circuit for the Firecomms transceiver. It assumes that the LVDS device (FPGA or ASIC) does not have internal termination. Both Optical transmitter and receiver require a common mode voltage of 1.25V for optimum operation.

APPLICATION CIRCUIT FOR A CML INTERFACE

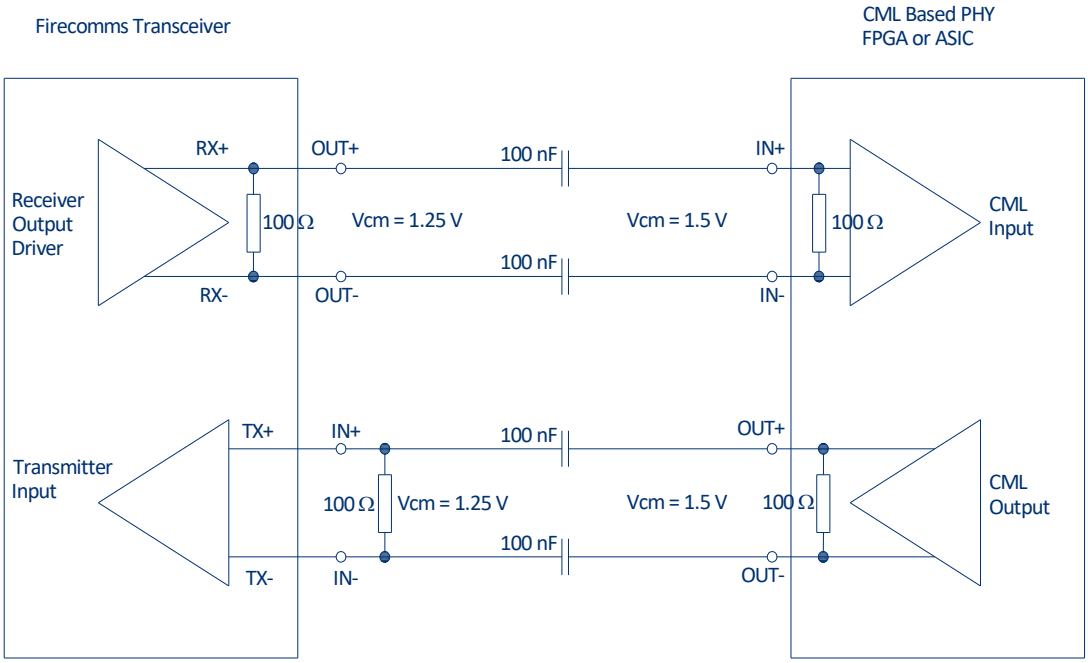

FIGURE 6
This is the general AC coupled CML interface circuit for the Firecomms transceiver. It assumes that the CML device has internal termination. The CML side of the coupling capacitors has a common mode voltage of 1.5 V.

APPLICATION CIRCUIT FOR AN LVPECL INTERFACE

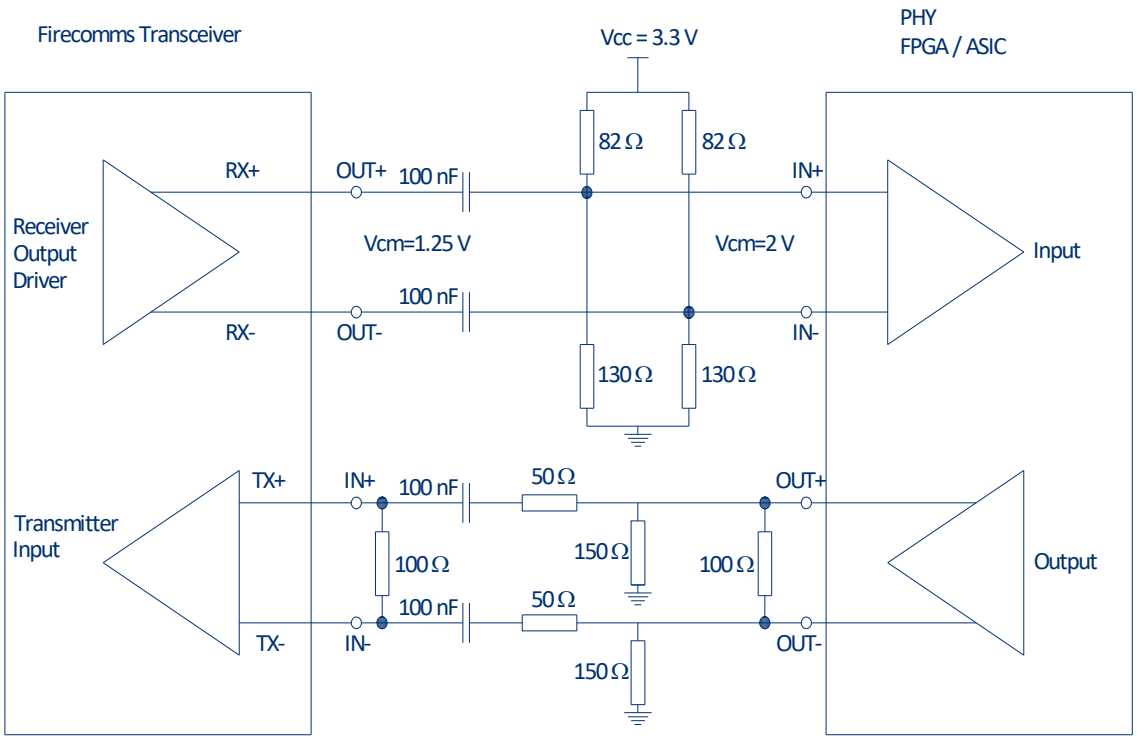

FIGURE 7
This is the general AC coupled LVPECL interface circuit for the Firecomms transceiver. It assumes that the PHY/FPGA/ASIC device does not have internal termination. The resistor network sets the Common mode voltage of 2V for the LVPECL application circuit.

The Firecomms transceiver can be interfaced to standard LVPECL devices such as 100 Mbps Fast Ethernet PHY IC's. AC coupling is important to ensure the correct common mode voltage. The optical receiver is a CMOS device and its output stage has a common mode of 1.25V. By AC coupling this to a standard LVPECL resistor network (82/130 Ω) the common mode is shifted to 2V and the correct VOH to VOL voltage swing is achieved.

The 100 nF AC coupling capacitors are ideal for high speed operation (100 to 200 Mbps). For lower data rates these should be increased as appropriate.

As Ethernet PHY IC's often differ in the design of their interface circuits, we recommend that the reader contact Firecomms application support who can advise on the exact circuit that will work best with leading PHY suppliers, for example Micrel/Microchip, Marvell, Realtek, TI and IC Plus.

Firecomms can also provide support with interfaces to FPGA's from Xilinx, Altera, Lattice and others.

SPECIFICATIONS

Table 4
REGULATORY COMPLIANCE

Parameter	Symbol	Standard	Level
Storage Compliance	MSL	J-STD-020E	2a (4-week floor life)
Restriction of Hazardous Substances Directive	RoHS	Directive 2011/65/EU	Certified compliant
Eye Safety		IEC 60825-1	LED Class 1

Table 5
ABSOLUTE MAXIMUM RATINGS

These are the absolute maximum ratings at or beyond which the component can be expected to be damaged
Notes:
1. *260 °C for 10 seconds, one time only, at least 2.2 mm away from lead root*

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T_{stg}	-40	+85	°C
Operating Temperature	T_{op}	-40	+85	°C
Soldering Temperature [1]	T_{sld}		+260[1]	°C
Supply Voltage	V_R	-0.5	3.6	V
Receiver Optical Overload	P_{OL}		0	dBm

SPECIFICATIONS

Table 6
TRANSMITTER ELECTRICAL AND OPTICAL CHARACTERISTICS

Test Conditions:

1. *Test data was validated over the full temperature range of -40 °C to +85 °C, and over the supply range of 3 V to 3.6 V.*
2. *Test data represents operation at the maximum data rate of 250 Mbps using a PRBS7 test pattern unless otherwise stated*
3. *Average optical power is measured when coupled into 0.5 m of a 1 mm diameter 0.5 NA POF*
4. *Typical Ethernet applications will run at 100 Mbps of 4B5B encoded date which is equivalent to 125 MBd*
5. *Typical FPGA applications will run at 200 Mbps of 8B10B encoded data which is equivalent to 250 MBd.*

Parameter	Symbol	Min	Typical	Max	Unit	Test Condition
DC Supply Voltage	Vcc	3.0	3.3	3.6	V	
Operating Current Consumption	Icc		37	52	mA	
Sleep State Current Consumption	I_{Sleep}		20	40	µA	< 30 dBm of light
Data Rate		10		250	Mbps	See encoding [2], [4], [5]
Data Input Capacitance	C_{IN}			5	pF	
Data Input Resistance (Single-Ended)	R_{IN}		5		kΩ	
Input Common-Mode Range	$V_{IN-BIAS}$	GND+0.8		V_{CC}-0.8	V	
Input Voltage Swing	$V_{IN-SWING}$	100		1200	mV	
Minimum Differential Voltage Swing to Ensure Wake-Up	Wake-up Input	50			mV	
Wake-Up Time Delay			5	80	µs	
Optical Power OFF Delay		0.02		20	µs	
Peak Wavelength	λ_{peak}	640	660	670	nm	
Spectral Bandwidth (FWHM)	Δλ		23	30	nm	
Average Optical Power	P	-10		-2.0	dBm	[3]
Rise Time (20 % - 80 %)	t_R		2.0	2.8	ns	
Fall Time (80 % - 20 %)	t_F	0.3		0.6	ns	
Optical Modulation Amplitude	OMA	160	590	1250	µW	
Total Jitter				1.6	ns	

SPECIFICATIONS

Table 7
RECEIVER ELECTRICAL AND OPTICAL CHARACTERISTICS

Test Conditions:

1. *Test data was validated over the full temperature range of -40 °C to +85 °C, and over the supply range of 3 V to 3.6 V*
2. *Test data represents operation at the maximum data rate of 250 Mbps using a PRBS7 test pattern unless otherwise stated*
3. *Average optical power was coupled from a minimum 0.5 m length of 1 mm diameter core and 0.5 NA step index POF*
4. *Measured by an oscilloscope with 50 Ohm termination for each data input line or using a 100 Ohm terminated differential probe.*
5. *Typical Ethernet applications will run at 100 Mbps of 4B5B encoded date which is equal to 125 MBd*
6. *Typical FPGA applications will run at 200 Mbps of 8B10B encoded data which is equal to 250 MBd.*

Parameter	Symbol	Min	Typical	Max	Unit	Test Condition
DC Supply Voltage	Vcc	3.0	3.3	3.6	V	
Data Rate		10		250	Mbps	See encoding [2],[5],[6]
Operating Current Consumption	Icc	18	22	30	mA	
Sleep State Current Consumption	I_{Sleep}	2	7	15	µA	
Output Impedance Between D and $\underline{D}$			100		Ohm	
Offset Common Mode Voltage	V_{cm}	1.2	1.25	1.3	V	
Output Differential Voltage Swing		650	800	950	mV	[4]
Receivable Average Optical Power Sensitivity				-24	dBm	
Maximum Allowed Average Optical Power				0	dBm	
Rise Time (10 % - 90 %)			1.0	2.5	ns	
Fall Time (90 % - 10 %)			1.0	2.0	ns	
Wake Up Time from Sleep State			10	100	µs	

MECHANICAL DATA

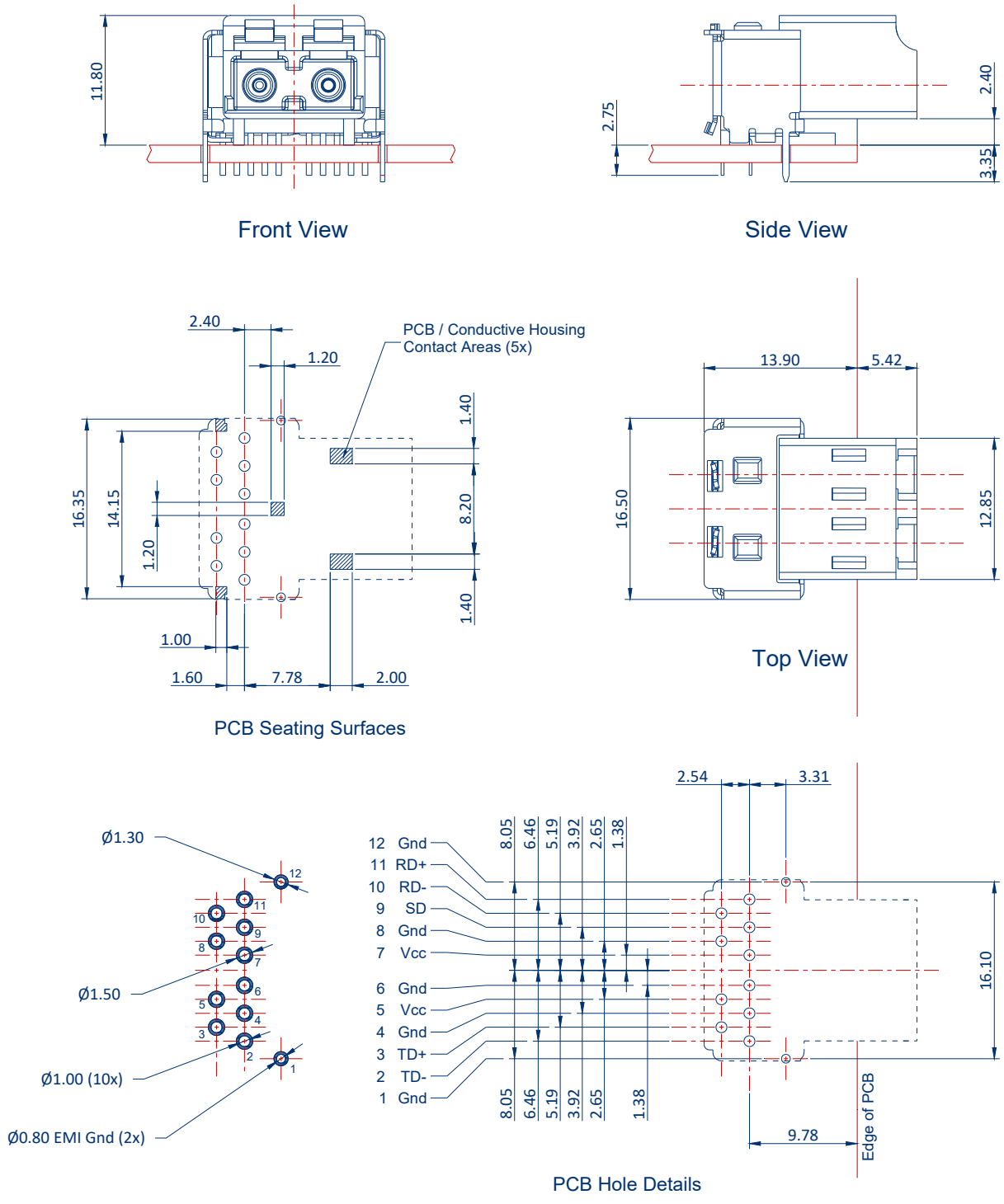

FIGURE 8
Mechanical dimensions of the product, and PCB footprint, which is a top view
General dimensional tolerance is ± 0.2 mm

Note: The plastic housing of the FB2M5LVR LC connector is made from an electrically conductive fibre-filled plastic material. Electrically conductive traces on the connector seating surface of the printed circuit board should not run underneath the connector housing. If it is necessary to run electrically conductive traces underneath the connector, their positions must not coincide with the PCB seating surfaces shown above.

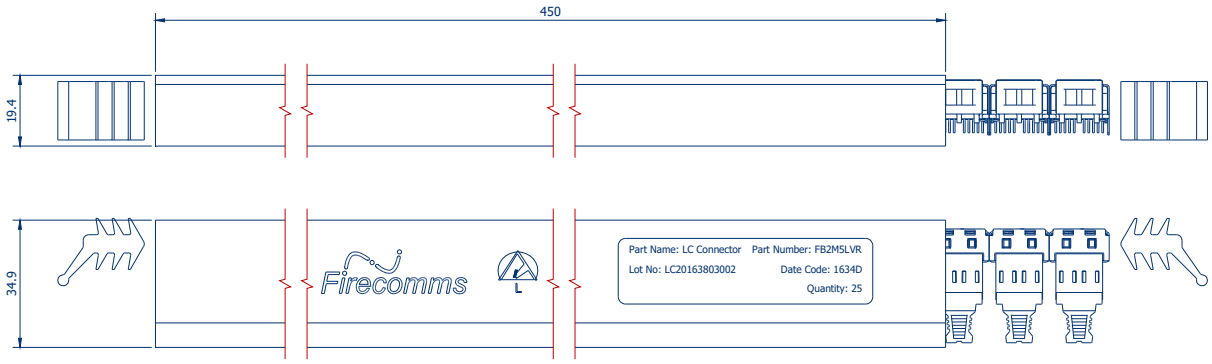

FIGURE 9
Packing tube for Firecomms FB2M5LVR Optical LC Transceivers

PART HANDLING

The transceivers are tested for handling in static-controlled assembly processes (HBM). Cleaning, degreasing and post solder washing should be carried out using standard solutions compatible with both plastics and the environment. For example, recommended solutions for degreasing are alcohols (methyl, isopropyl and isobutyl). Acetone, ethyl acetate, phenol or similar solution based products are not permitted.

In the soldering process, non-halogenated water soluble fluxes are recommended. These components are not suitable for use in reflow solder processes (infrared/vapor-phase reflow). The dust plug should remain in place during soldering, washing and drying processes to avoid contamination of the active optical area of each connector.

The Moisture Sensitivity Level (MSL) classification of this device is 2a according to JEDEC J-STD-020E.
The shelf life of an unopened MBB (Moisture Barrier Bag) is 24 months at < 40°C and < 90 % R.H.
Once the Moisture Barrier Bag is opened the devices can be either

a) Stored in normal factory conditions < 30 °C and < 60 % R.H. for a maximum of 672 hours (4 Weeks) prior to soldering.
b) Stored at < 10 % R.H. (Dry Cabinet).

PACKING INFORMATION

Components are packed in PVC anti-static tubes in moisture barrier bags. Bags should be opened only in static-controlled locations, and standard procedures should be followed for handling moisture sensitive components.

Components per Tube		25
	Tube Length	450 mm
	Tube Width	34.9 mm
	Tube Height	19.4 mm
Tubes per Bag		10
Bags per Inner Carton		1
	Inner Carton Length	588 mm
	Inner Carton Width	147 mm
	Inner Carton Height	82 mm
Weight per Inner Carton, Complete		1.95 kg
Components per Inner Carton		250
Inner Cartons per Outer Carton		4
	Outer Carton Length	600 mm
	Outer Carton Width	310 mm
	Outer Carton Height	195 mm
Weight per Outer Carton, Complete		8.10 kg
Components per Outer Carton		1,000