

# OBSOLETE

\* For new designs please see part numbers: FB2M5KVR (2.2 mm POF)

## 650 nm 250 Mbps Transceiver in OptoLock® Termination IDL300T-XXX



### LVDS I/O

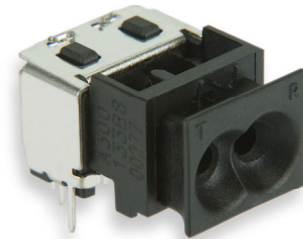
#### FEATURES

- Simple low-cost termination solution for 2.2 mm jacketed POF cables without a plug
- Compatible with 8B/10B encoding schemes: 250 Mbps NRZ symbol rate
- Resonant Cavity LED (RCLED) at red 650 nm with small emission aperture suitable for POF
- RCLED reliability tested to over 400,000 hours lifetime
- Integrated CMOS driver IC for RCLED
- High sensitivity CMOS receiver IC and PIN diode for one-step light to digital conversion
- Integrated optics to efficiently focus and direct light
- Low power consumption with power saving features
- -20° to +85°C operating range
- RoHS compliant

#### APPLICATIONS

Table 1 APPLICATIONS	
Application	Medical device, Consumer and Robotic FPGA-FPGA Links.
Standard	LVDS Bus
Distance	50 meters Step Index POF <sup>[1]</sup> 50 meters PCS 200µm glass fiber
Speed	250 Mbps

Note: 1. Depending on the installation conditions.



#### DESCRIPTION

Firecomms OptoLock® transceiver has a small form factor housing which combines a pair of Firecomms fiber optic components to provide instant termination for bare Plastic Optical Fiber (POF). This POF port significantly simplifies the optical connection and as a consequence reduces time spent in maintenance of equipment.

This version of OptoLock® houses a pair of Fiber Optic Transceivers (FOTs) designed to provide fast data links over POF between high-speed IC's using an LVDS bus. The FOTs are compatible with low-voltage differential signalling (LVDS) for seamless integration into existing logic bus structures and are ideal for use with FPGAs, ASICs, ARM processors or high speed micro-controllers.

The transceiver has electrical power saving features. In the transmitter, the driver IC goes into a sleep state and the RCLED is switched off when there is no data or pulse toning on the input bus. Similarly, if there is no optical signal present, the RX IC will switch into a sleep mode with RX power consumption reduced to a value of 25uA or less.

The Receiver has a signal detect output which is an open-collector CMOS output providing a link diagnostic detection function to feedback the link status to the processor or micro-controller.

OptoLock® is protected by U.S. patents 7,597,485 and 7,905,665, Chinese patents 101501545 A and 102135650 B and other international patents.

#### IDL300T-XXX Revision C

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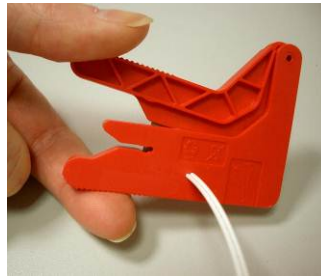


## TERMINATION STEPS

To terminate the POF cable into OptoLock®, the end of the cable is cut cleanly, and the two strands are separated. One strand is inserted into each of two holes in the termination housing, which is then pressed closed to hold the POF in place. These steps are shown here.



**FIGURE 1**  
Slice the POF cable.



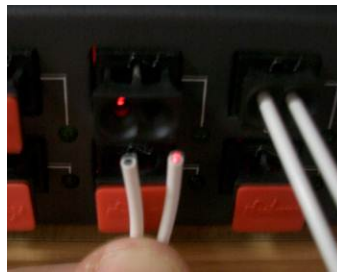
**FIGURE 2**  
Cut a clean finish to the end.



**FIGURE 3**  
Split the duplex POF.



**FIGURE 4**  
Identify the POF core that is lit.



**FIGURE 5**  
Present the lit core to the dark OptoLock® side.



**FIGURE 6**  
Insert both strands into OptoLock®.



**FIGURE 7**  
Push home to lock the clamp.

The following photographs show several OptoLock® transceivers in use in a high speed communications switch.



**FIGURE 8**  
Side view of OptoLock® transceivers



**FIGURE 9**  
Front view of OptoLock® transceivers

## SPECIFICATIONS

Table 2 ABSOLUTE MAXIMUM RATINGS				
<i>These are the absolute maximum ratings at or beyond which the FOT can be expected to be damaged.</i>				
Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	$T_{stg}$	-40	85	°C
Operating Temperature	$T_{op}$	-20	85	°C
Soldering Temperature <sup>[1]</sup>	$T_{slid}$		260	°C
Supply Voltage	$V_R$	-0.5	4.5	V
Receiver Optical Overload	$P_{OL}$		0	dBm
Storage Conditions (Moisture Level Sensitivity)	MSL		2a	J-STD-020D

Notes:

1. 260°C for 10 sec, 1 time only, at least 2.2 mm away from lead root.

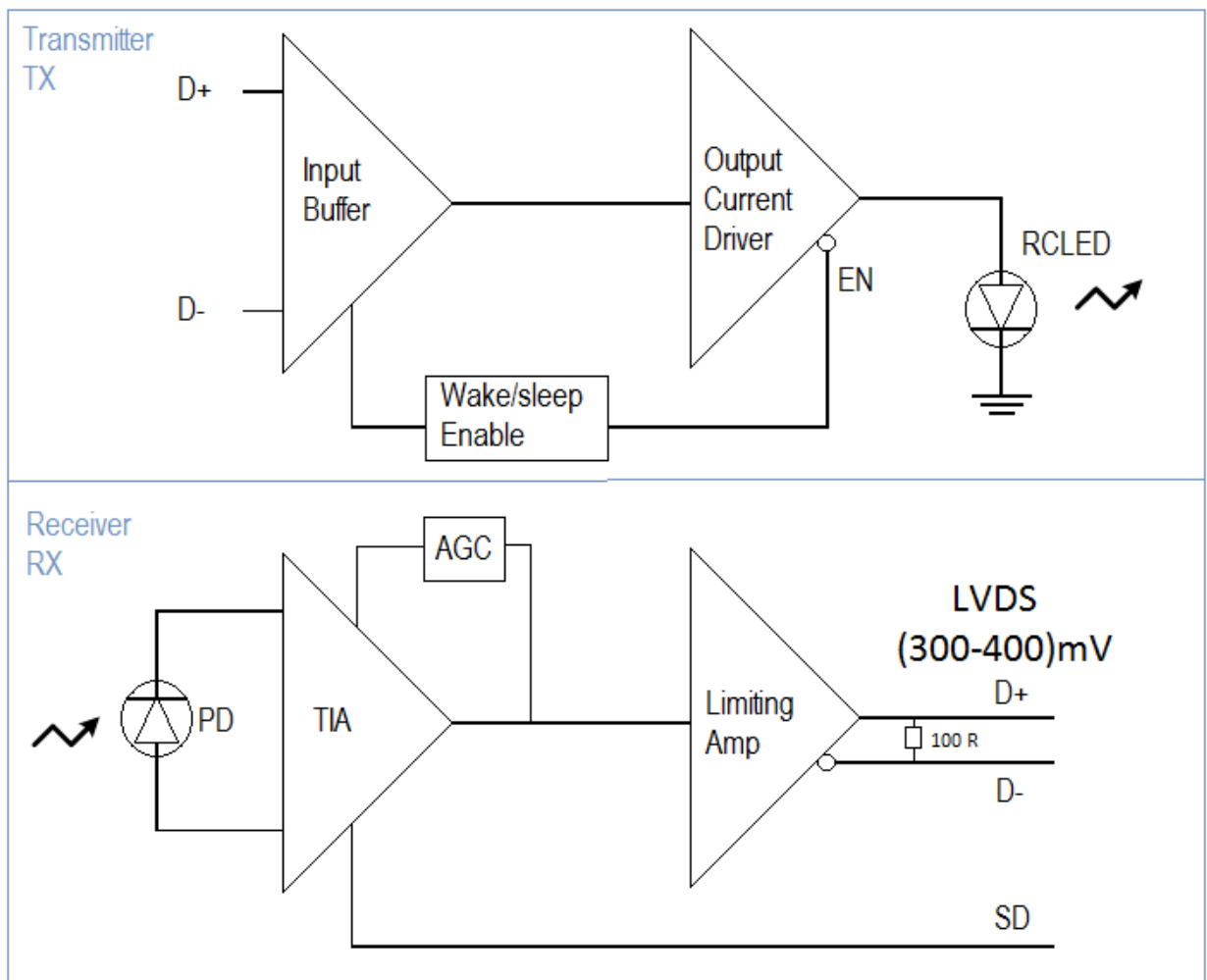


FIGURE 10  
OptoLock® transceiver electronic block diagram

## SPECIFICATIONS (continued)

**Table 3**  
**TRANSMITTER ELECTRICAL AND OPTICAL CHARACTERISTICS**

**Test Conditions:**

1. Test data was validated over the full temperature range of -20°C to +85°C, and over the supply range of 3V to 3.6V.
2. Test data represents operation at the maximum data rate of 250 Mbps using a PRBS7 test pattern (8B/10B encoding) unless otherwise stated.
3. Optical power is measured when coupled into 0.5 m of a 1 mm diameter 0.5 NA plastic fiber.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
DC Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Operating Current Consumption	I <sub>CC</sub>		37	52	mA
Sleep State Current Consumption	I <sub>Sleep</sub>		20	40	μA
Data Rate	Baud Rate	10		250	Mbps
Data Input Capacitance	C <sub>IN</sub>			5	pF
Data Input Resistance (Single-Ended)	R <sub>IN</sub>		5		kΩ
Input Common-Mode Range	V <sub>IN-BIAS</sub>	GND+0.8		V <sub>CC</sub> -0.8	V
Input Voltage Swing	V <sub>IN-SWING</sub>	100		1200	mV
Minimum Differential Voltage Swing to Ensure Wake-Up	Wake-up Input	50			mV
Wake-Up Time Delay			5	80	μs
Optical Power OFF Delay		0.02		20	μs
Peak Wavelength	λ <sub>peak</sub>	640	660	670	nm
Spectral Bandwidth (FWHM)	Δλ		23	30	nm
Average Optical Power <sup>[3]</sup>	P	-10		-2.0	dBm
Optical Rise Time (20%-80%)	t <sub>R</sub>		2.0	2.8	ns
Optical Fall Time (80%-20%)	t <sub>F</sub>	0.3		0.6	ns
Optical Modulation Amplitude (OMA)	OMA	160	590	1250	μW
Total Jitter				1.6	ns

## SPECIFICATIONS (continued)

**Table 4**  
**RECEIVER CHARACTERISTICS**

*Test Conditions:*

1. Test data was validated over the full temperature range of -20°C to +85°C, and over the supply range of 3V to 3.6V.
2. Test data represents operation at the maximum data rate of 250 Mbps using a PRBS7 test pattern (8B/10B encoding) unless otherwise stated.
3. Optical power was coupled from a minimum 0.5 m length of 1 mm diameter core and 0.5 NA step index plastic optic fiber.

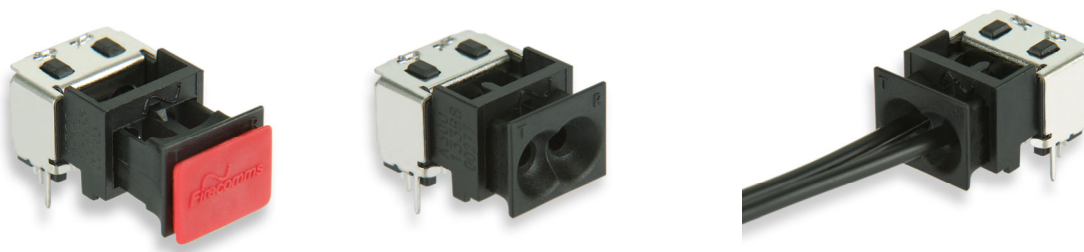
Parameter	Symbol	Minimum	Typical	Maximum	Unit
DC Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Operating Current Consumption	I <sub>CC</sub>	34	36	40	mA
Sleep State Current Consumption	I <sub>Sleep</sub>	2	20	25	μA
Output Impedance Between D and $\bar{D}$			100		Ohm
Offset Common Mode Voltage	V <sub>OCM</sub>		1.2		V
Output Differential Voltage Swing		300	350	400	mV
Receivable Optical Power Sensitivity			-24	-22	dBm
Maximum Allowed Optical Power				0	dBm
Rise Time (10%-90%)			1.0	2.5	ns
Fall Time (90%-10%)			1.0	2.0	ns
Wake Up Time from Sleep State			10	100	us

## SPECIFICATIONS (continued)

Table 5 TRANSCEIVER PIN DESCRIPTION		
Pin	Name	Symbol
TRANSMITTER		
1	EMI-GND	GND
2	Data Input (Negative)	TD-
3	Data Input (Positive)	TD+
4	Ground Pin <sup>[1]</sup>	GND
5	DC Power Input Pin	Vcc
6	Ground Pin <sup>[1]</sup>	GND
RECEIVER		
7	DC Power Input Pin	Vcc
8	Ground Pin <sup>[1]</sup>	GND
9	Signal Detect Output	SD
10	Data Output (Negative)	RD-
11	Data Output (Positive)	RD+
12	EMI-GND	GND

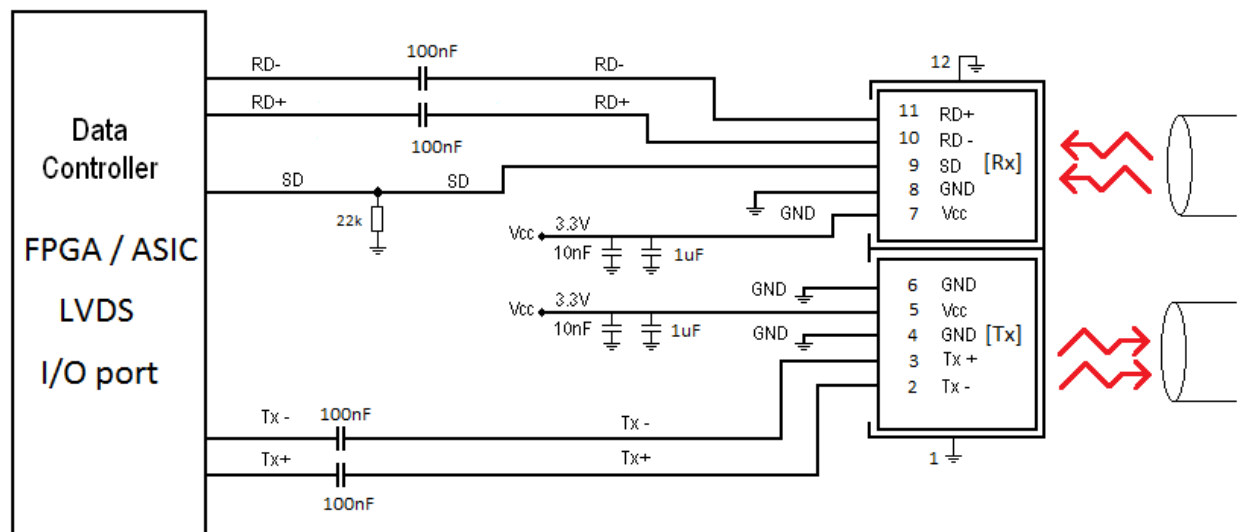
Notes:

1. NB: both ground pins must be connected to the ground plane on the PCB. These pins are not connected internally.



**FIGURE 11**  
OptoLock<sup>®</sup> shown with dust cap, as open for fiber, and with fiber inserted.

## APPLICATION CIRCUIT

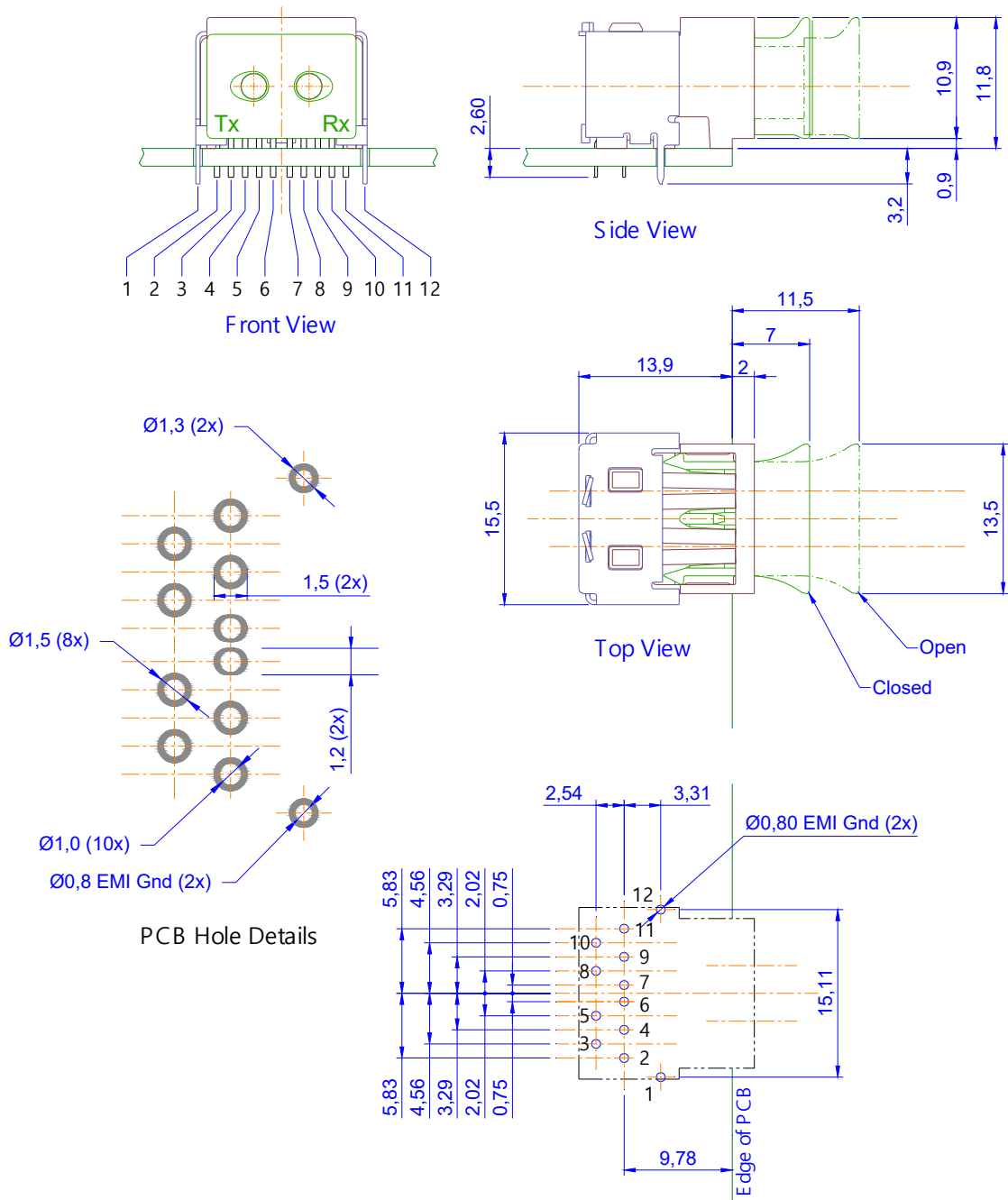


**FIGURE 12**  
Interface circuit schematic to AC couple to a PHY, FPGA , ASIC, ARM processor.

### Notes:

1. Signal Detect is a CMOS Open Collector Output. It pulls up to High (Vcc) when an optical signal is present at the receiver and pulls down to logic Low (ground) when there is no optical data present at the photo-diode input to the receiver.
2. The transmitter (TX) and receiver (RX) are electrically shielded from each other to prevent crosstalk. To be effective this shield must be grounded
3. Both GND pins of the TX FOT must be connected to GND (they are not connected internally).
4. Power line capacitors should be located as close as possible to the FOT's DC power PINs.
5. The data lines are impedance-matched differential pairs. The PCB layout for these tracks must comply to IEEE/IEC standards for high-speed data and impedance matching.

## MECHANICAL DATA



**FIGURE 13**  
**Mechanical dimensions of the OptoLock® connector and PCB footprint, which is a top view.**  
**General dimensional tolerance is ±0.2mm.**



## PACKING INFORMATION

Components are packed in PVC anti-static tubes in moisture barrier bags. Bags should be opened only in static-controlled locations, and standard procedures should be followed for handling moisture sensitive components.

Table 6 PACKING INFORMATION		
Components per Tube		25
	Tube Length	440 mm
	Tube Height	20 mm
	Tube Depth	31 mm
Tubes per Bag		10
Bags per Inner Carton		1
	Inner Carton Length	590 mm
	Inner Carton Height	85 mm
	Inner Carton Depth	145 mm
Weight per Inner Carton, Complete		1.8 Kg
Components per Inner Carton		250
Inner Cartons per Outer Carton		4
	Outer Carton Length	600-640 mm
	Outer Carton Height	300 mm
	Outer Carton Depth	200-285 mm
Weight per Outer Carton, Complete		8.6 Kg
Components per Outer Carton		1,000

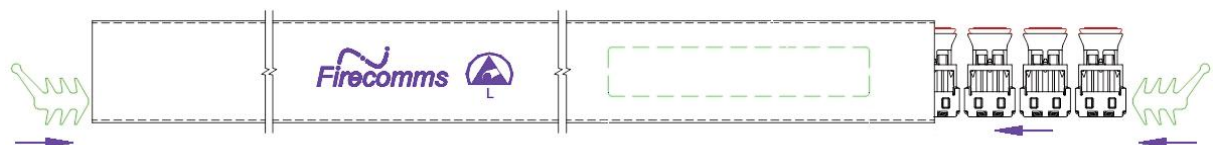


FIGURE 14: Packing tube for the Firecomms transceiver

## ORDERING INFORMATION

Table 7 ORDERING INFORMATION		
Part Number	Name	Description
IDL300T-220	250Mb OptoLock®, 2.2 mm, Black	650 nm RCLED-Based Transceiver, Color Black, with termination for Bare POF Cable 2.2 mm Diameter
IDL300T-229	250Mb OptoLock®, 2.2 mm, White	650 nm RCLED-Based Transceiver, Color White with termination for Bare POF Cable 2.2 mm Diameter
IDL300T-150	250Mb OptoLock®, 1.5 mm, Black	650 nm RCLED-Based Transceiver, Color Black, with termination for Bare POF Cable 1.5 mm Diameter
IDL300T-159	250Mb OptoLock®, 1.5 mm, White	650 nm RCLED-Based Transceiver, Color White, with termination for Bare POF Cable 1.5 mm Diameter

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